WHAT IS CLAIMED IS:

1. A Read-Only Memory (ROM) instance, comprising:

a plurality of ROM cells organized as an array having M rows and N columns, wherein said M rows are grouped into K banks; and

a partitioned source line associated with each of said N columns, said partitioned source line including a plurality of source line segments, each segment being decodable based on a Bank Select (BS) signal that is operable to select a bank and on a column address for selecting a particular column of said N columns.

2. The ROM instance as set forth in claim 1, wherein each segment of said partitioned source line is individually precharged to a predetermined level.

3. The ROM instance as set forth in claim 2, wherein a particular segment of said partitioned source line is operable to be driven low upon commencing a memory access operation, provided a ROM cell associated with said particular segment is selected.

4. The ROM instance as set forth in claim 3, wherein each of said N columns is associated with a global bitline.

5. The ROM instance as set forth in claim 4, wherein said BS signal is generated based on a plurality of row address signals supplied to said ROM instance.

6. The ROM instance as set forth in claim 5, wherein each bank is associated with a local circuit portion including precharge circuitry for precharging N source line segments corresponding to said grouping.

7. The ROM instance as set forth in claim 6, wherein said local circuit portion includes pull-down circuitry for driving low a particular one of said N source line segments based on a column address.

8. The ROM instance as set forth in claim 5, wherein each ROM cell comprises a Field Effect Transistor (FET) device whose source is coupled to said partitioned source line.

9. The ROM instance as set forth in claim 5, wherein each of said banks comprises one of 16, 32, 64, 128, 256, and 512 rows.

10. The ROM instance as set forth in claim 5, wherein each source line segment is decoded by a local source line decoder circuit.

11. A memory compiler for compiling at least one Read-Only Memory (ROM) instance, comprising:

a code portion for generating a plurality of ROM cells organized as an array having M rows and N columns, wherein said M rows are grouped into K row banks and each of said N columns is associated with a partitioned source line that comprises a plurality of source line segments corresponding to said K row banks of said array;

a code portion for generating a local circuit portion associated with each row bank, said local circuit portion including local precharge circuitry and local pull-down circuitry;

a code portion for generating a plurality of local source line decoder circuits corresponding to said row banks, each local source line decoder circuit operating responsive to at least one Bank Select (BS) signal and at least a portion of a column address for selecting a particular column of said N columns; and

a code portion for generating a global input/output circuit block associated with said ROM memory instance for sensing data on global bitlines corresponding to said N columns.

12. The memory compiler for compiling at least one ROM memory instance as set forth in claim 11, wherein said at least one BS signal is generated based on a plurality of row address signals.

13. The memory compiler for compiling at least one ROM memory instance as set forth in claim 11, wherein said local pull-down circuitry comprises N-channel field-effect transistor (N-FET) devices.

14. The memory compiler for compiling at least one ROM memory instance as set forth in claim 11, wherein each of said row banks comprises one of 16, 32, 64, 128, 256, and 512 rows.

15. The memory compiler for compiling at least one ROM memory instance as set forth in claim 11, wherein said pull-down circuitry is operable to drive low a particular one of said source line segments upon commencing a memory access operation.

16. The memory compiler for compiling at least one ROM memory instance as set forth in claim 11, further comprising a code portion for generating a reference I/O block associated with said ROM memory instance.

17. The memory compiler for compiling at least one ROM memory instance as set forth in claim 11, wherein each ROM cell comprises a Field Effect Transistor (FET) device whose source is coupled to said partitioned source line.

18. A memory operation method associated with a Read-Only Memory (ROM) instance, said ROM instance having a plurality of ROM cells organized in an array having M rows and N columns, wherein each of said N columns is associated with a precharged source line that is partitioned into a number of source line segments based on a number of row banks of said array:

providing row address and column address signals for accessing a ROM cell location;

based on said row address signals corresponding to said ROM cell location's row, generating a Bank Select (BS) signal;

based on said column address signals and said BS signal, deactivating a source line segment associated with said ROM cell location, thereby developing a read voltage differential on a global bitline associated therewith;

sensing said read voltage differential by a global sense amplifier (sense amp) circuit for outputting; and

upon substantial completion of said sensing, precharging said source line segment.

19. The memory operation method associated with a ROM instance as set forth in claim 18, wherein said source line segment is deactivated by a pull-down control signal generated by a local source line decoder circuit that is associated with a selected row bank.

20. The memory operation method associated with a ROM instance as set forth in claim 19, wherein said selected row bank comprises one of 16, 32, 64, 128, 256, and 512 rows.